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(54) METHOD OF MANUFACTURING METAL OXIDE TRANSISTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To manufacture an FET by using a metal oxide semiconductor.

SOLUTION: A gate insulating film 32 of SiO₂ is formed on an Si substrate 31. Zn(OAc)₂·4H₂O is suspended in isopropanol and the gate insulating film 32 is coated with this suspension. A channel layer 33 of ZnO is formed by thermal treatment and a source electrode 34 and a drain electrode 35 are formed thereon.

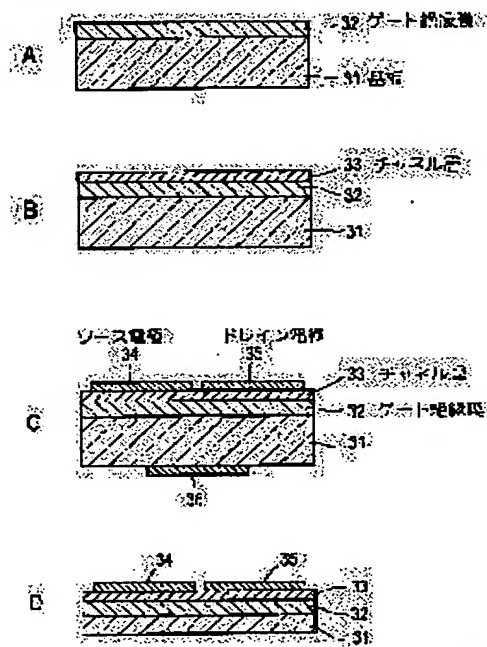


図1

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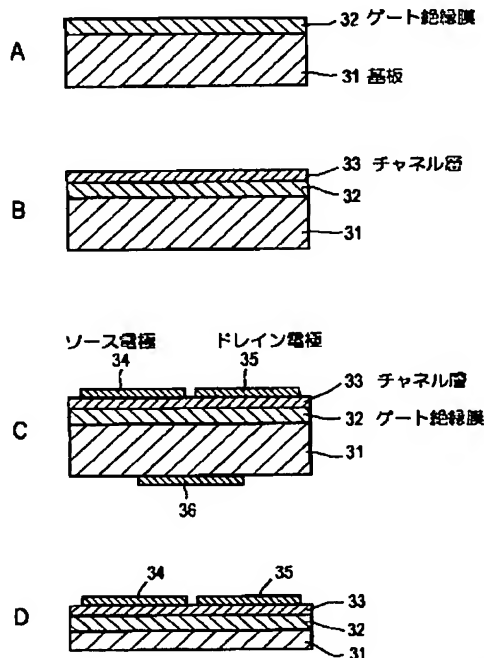
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(54) 【発明の名称】 金属酸化物トランジスタの製造方法

(57) 【要約】

【課題】 金属酸化物半導体を用いてFETを作製する。

【解決手段】 Si基板31上にSiO₂膜のゲート絶縁膜32を形成し、Zn(OAc)₂・4H₂Oをイソプロパノールに懸濁し、これをゲート絶縁膜32上にコーティングした後、加熱処理してZnOからなるチャネル層33を形成し、その上にソース電極34とドレイン電極35を形成する。



【特許請求の範囲】

【請求項 1】 基板上にゲート絶縁膜を形成し、そのゲート絶縁膜上に n 形又は p 形金属酸化物半導体薄膜を溶液法で作ってチャンネル層を形成し、そのチャンネル層上にソース電極及びドレイン電極を形成することを特徴とする金属酸化物トランジスタの製造方法。

【請求項 2】 上記溶液法によるチャンネル層の形成は、上記金属酸化物が析出できる範囲で比較的低い温度で上記金属酸化物層を形成し、その後、上記温度より高い温度で上記金属酸化物を酸化させて上記金属酸化物半導体薄膜を得ることを特徴とする請求項 1 記載の金属酸化物トランジスタの製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 この発明は金属酸化物半導体を用いて金属-絶縁膜-半導体構造の電界効果形トランジスタを製造する方法に関する。

【0002】

【従来の技術】 従来のトランジスタは単結晶シリコンに不純物を拡散させ気相成長させたり、あるいは化合物半導体を気相成長させて p-n 接合を形成して製造するものが主流である。これらの場合は排ガスの処理に大きな設備と、処理費用を要した。一方、ゾルーゲル (Sol-Gel) 法に代表される溶液法により金属酸化物半導体を作製すれば排ガス処理の問題がなく、比較的簡単な設備で安価に作ることが可能である。しかし酸化物半導体は、一般に移動度が低いため、Si、Ge、化合物半導体と比較して扱いにくい欠点があった。またゾルーゲル法によって作製された薄膜はポーラスであることが多く、ガスセンサのように膜表面での吸着反応を利用することは試みられているが、厚さ方向の電導現象はほとんど利用されていない。

【0003】 例えば図 5 に示すように基板 11 上に、NiO などの n 形金属酸化物層 12 を形成し、その上に TiO などの p 形金属酸化物層 13 を溶液法により形成し、更にその上に NiO などの n 形金属酸化物層 14 を溶液法により形成して接合形トランジスタを構成することが考えられる。しかし各金属酸化物層の形成ごとに、600~800℃程度の高温加熱を必要とするため、p 形金属酸化物層 13 を形成する際に、その下の n 形金属酸化物層 12 と p 形金属酸化物層 13 との境界に両層の複合酸化物膜 15 が生成され、また n 形金属酸化物層 14 を形成する際にその n 形金属酸化物層 14 と p 形金属酸化物層 13 との境界に両層の複合酸化物膜 16 が生成され、しかも先に形成された複合酸化物膜 15 が成長して、その膜厚が厚くなる。この複合酸化物膜、特に 15 が完全な絶縁物となり、電子や正孔が移動することができず、トランジスタとして作用させることが困難である。

【0004】 あるいは図 6 に示すように、シリコン基板 11 上に NiO のような n 形金属酸化物層よりなるチャンネル層 17 を溶液法により形成し、そのチャンネル層 17 上の一部に SiO₂ などのゲート絶縁膜 18 を溶液法により形成し、ゲート絶縁膜 18 上にゲート電極 19 を、ゲート絶縁膜 18 の両側においてチャンネル層 17 上にソース電極 21、ドレイン電極 22 を形成して、M-I-S 構造の電界効果形トランジスタを構成することも考えられる。この場合は、ゲート絶縁膜 18 の形成後に、高温に加熱することがないため、チャンネル層 17 とゲート絶縁膜 18 の境界に生じる複合酸化物膜はそれ程厚いものにはならない。しかし、チャンネル層 17 上に、ゲート絶縁膜 18 を溶液法で作る場合、絶縁性の良好なものを作ることが困難であった。

【0005】

【発明が解決しようとする課題】 以上述べたように、溶液法により金属酸化物半導体を作製すれば製造設備が比較的簡単な半導体素子を作ることができるが、従来においてはトランジスタを作ることが困難であった。

【0006】

【課題を解決するための手段】 この発明によれば基板上にゲート絶縁膜を形成し、そのゲート絶縁膜上に n 形又は p 形金属酸化物半導体薄膜を溶液法で作ってチャンネル層を形成し、そのチャンネル層上にソース電極及びドレイン電極を形成する。上記溶液法によるチャンネル層の形成は、比較的低い温度で金属酸化物を析出させた後、その温度より高い温度で析出した金属酸化物を酸化させて金属酸化物半導体薄膜を得ることが好ましい。

【0007】

【発明の実施の形態】 図 1 にこの発明の実施例を示す。先ず例えば (100) 単結晶シリコン (n 形、 $1.4 \times 10^{-2} \Omega \text{cm}$) の基板 31 を用意し、その基板 31 上にゲート絶縁膜 32 を形成する。このゲート絶縁膜 32 は基板 31 を熱酸化して SiO₂ 膜を形成して作ることができる。あるいはスパッタリングにより SiO₂ 膜を形成してもよい。ゲート絶縁膜 32 の厚さは例えば 130 nm とする。

【0008】 このゲート絶縁膜 32 上に n 形又は p 形の金属酸化物半導体薄膜を溶液法により形成してチャンネル層 33 とする (図 1B)。例えば有機金属液体として Zn(OAc)₂ · 4H₂O を使い、これをイソプロパノール (アルコールの一種) に懸濁させ、Zn に対し等モルのジエタノールアミンを加水分解抑止剤として添加して溶解し、更に 2 倍モルの水を添加して 0.4 mol/l の溶液を調整する。この溶液をディップコーティング法、又はスプレー法、スピニング法によりゲート絶縁膜 32 上にコーティングする。ディップコーティングの場合、溶液中から 6 cm/分の引き上げ速度で基板 31 を引き上げると 1 回のコーティングで 20 nm の ZnO 膜が形成されるが、例えば ZnO の膜厚、つまり

チャネル層33の膜厚が40nmになるようにコーティングを行い、その後、600℃～900℃の温度で空气中又は酸素雰囲気中で加熱処理を行い、ZnOの膜、つまりチャネル層33を形成する。

【0009】次に図1Cに示すように、チャネル層33上に金属膜により、ソース電極34とドレイン電極35を形成して電界効果形トランジスタ(FET)を得る。必要に応じて基板31のゲート絶縁膜32と反対側にゲート電極36を形成する。基板31自体をゲート電極としてもよい。電極34、35、36は例えばAuの蒸着により、或いはITO(インジウム、スズ酸化膜)などの透明電極材の溶液法により形成する。

【0010】ゲート絶縁膜32の厚さは、ゲート絶縁膜32とチャネル層33との境界に複合酸化膜が生成される点から、100nm程度以上が好ましいが、チャネル制御が確実に行われる点から500nm以下がよい。チャネルはチャネル層33のゲート絶縁膜32と接して形成され、ソース電極34とドレイン電極35の間にこのチャネルを通して電流が流れるには、電流はチャネル層33の厚さ方向に流れて、電極からチャネルへまたチャネルから電極へ電流が流れることになる。この点からチャネル層33の厚さを100nm程度以上にすると、電子空乏層ができて電流が流れ難くなる。また10nm程度以下にするとチャネルとしての動作が良好に行わなくなるおそれがある。これらの点からチャネル層33の厚さは10～100nm程度がよい。

【0011】チャネル層33の形成時における加熱処理の温度を600℃以下にすると、ゲート絶縁膜32とチャネル層33との境界にZnOとSiO₂の複合酸化物膜Zn₂SiO₄が十分生成されないため、ゲート絶縁膜32とチャネル層33との密着性が悪くまたゲート絶縁膜32を通るゲート電流が増加し、つまり絶縁性が悪く、良好なトランジスタ特性は得難くなる。従って、加熱処理温度は600℃以上とする。一方加熱処理温度を900℃以上にすると、複合酸化物膜Zn₂SiO₄の厚さが厚くなり、ZnO(チャネル層33)の厚さが薄くなり過ぎ、ソース電極34とドレイン電極35間に電流が流れ難くなり、トランジスタ特性が得られなくなる。この点より酸化処理温度は900℃以下とする。

【0012】前記Zn(OAc)₂・4H₂Oを用いて作った、0.4mol/lのディップ溶液に、2回ディップコーティングし、600℃、700℃、800℃及び900℃でそれぞれ加熱処理を各60分行ってFETを作製した。ここで600℃で加熱処理とは、1回ディップコーティングを行い乾燥後600℃で30分間加熱処理を行い、再び1回ディップコーティングを行い乾燥後600℃で30分間加熱処理を行うことである。700℃、800℃及び900℃での各加熱処理も同様にして各30分間の加熱処理を2回行った。このようにして作製したFETのX線回折パターンを図2に示す。加熱

処理の温度が低い600℃ではZn₂SiO₄に基づくピークが確認できないが、ZnOに基づくピークは確認される。加熱処理温度が高くなるに従ってZn₂SiO₄に基づくピークが確認できるようになり、逆にZnOに基づくピークが小さくなり、900℃ではZn₂SiO₄に基づくピークが可成り大きく現われ、逆にZnOに基づくピークが可成り小さくなり、(100)ZnOに基づくピークはほぼなくなっている。

【0013】これら実験結果より、加熱処理を、ZnOを析出させるが、Zn₂SiO₄の生成を生じない低い温度、つまり600℃による加熱を行ってZnOを析出させ、結晶化させた後、900℃で加熱処理して、結晶化したZnOをSiO₂(ゲート絶縁膜)と反応させてZn₂SiO₄を薄く生成した。両加熱処理の合計時間を60分とした。この場合のサンプルのX線回折パターンは、Zn₂SiO₄に基づくピークの温度が、900℃のみで加熱処理した場合のそれよりも小さくなった。更に透過形電子顕微鏡により断面を観察した所、ZnOとZn₂SiO₄との明白な界面が観察でき、SiO₂、Zn₂SiO₄及びZnOの各膜厚はそれぞれ115.40及び45nmであった。Zn₂SiO₄とSiO₂との界面は非常に密着性が良いものとなっていることも確認された。

【0014】以上のことから加熱処理は酸化物半導体結晶が析出するが、その酸化物半導体結晶とゲート絶縁膜と反応しない温度で加熱し、酸化物半導体を析出結晶化させた後、これよりも高い温度で加熱して析出結晶化した半導体とゲート絶縁膜とを反応させる手法が好ましいことが理解される。2回ディップコーティングで各600℃10分の加熱処理と、900℃15分の加熱処理との合計35分の加熱処理を行って作製したZnO-FETのドレイン電流とゲート電流のゲート電圧に対する特性を測定した。その結果を図3に実線と破線でそれぞれ示す。この図から、ゲート電極への漏れ(ゲート電流)は少なく、トランジスタ特性が得られていることが理解される。

【0015】上述において基板31としては石英ガラス、Al₂O₃など他の材料でもよい。またゲート絶縁膜32としてはSiN₄、SiONなどを用いてもよい。更にチャネル層33としては、ZnOに限らず、TiO₂、BaO、TiBaOなどを用いてもよく、またn形金属酸化物半導体のみならず、NiO、CuO₂、Co₂O₃などのp形金属酸化物半導体を用いてもよい。なお図1Dに示すように基板31を切削又は化学的エッチングにより、ゲート絶縁膜32と反対側を削り、基板31の厚さを例えば0.05mm以下、つまり可視光が透過する程度以下にし、場合によっては全て除去し、ゲート絶縁膜32にITOなどの透明電極(ゲート電極)を付けて液晶駆動トランジスタとして使用できるようにすることもできる。つまり透明なFETとすること

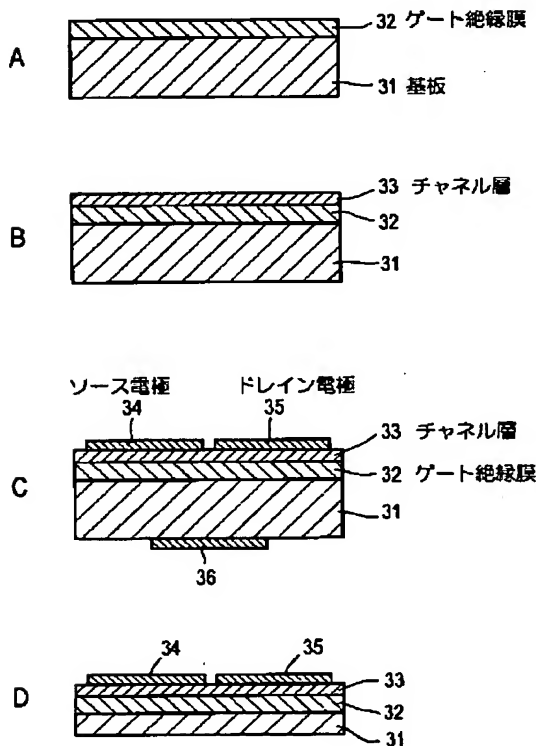
ともできる。また図4に示すように、図1Cに対し、ソース電極34、ドレイン電極35の形成面上に、これらの周縁部と一部重なるように酸化シリコンや強誘電体チタン酸バリウムなどの絶縁膜37を形成してチャネル層表面を流れる洩れ電流を減らすように少なくともチャネル層膜上に絶縁膜を溶液法で形成することが好ましい。

【0016】

【発明の効果】以上述べたようにこの発明によれば、チャネル層を溶液法により形成することにより、金属酸化物半導体をチャネル層としたFETを作製することができ、排ガス処理など大きな設備を必要とせず、比較的簡単な設備で製造することができる。

【図面の簡単な説明】

【図1】



【図4】

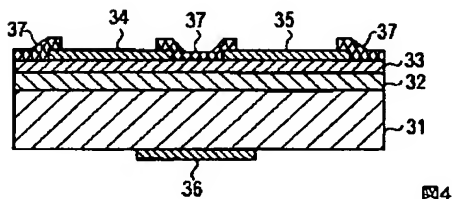


図4

【図1】この発明の実施例の製造工程を説明するための断面図。

【図2】各種加熱処理温度で作製したZnO-FETのX線回折パターンを示す図。

【図3】この発明方法で作ったZnO-FETのトランジスタ特性を示す図。

【図4】この発明方法で作られたトランジスタの例を示す断面図。

【図5】従来技術で考えられる接合形金属酸化物半導体トランジスタを示す断面図。

【図6】従来技術で考えられる金属酸化物半導体FETを示す断面図。

【図2】

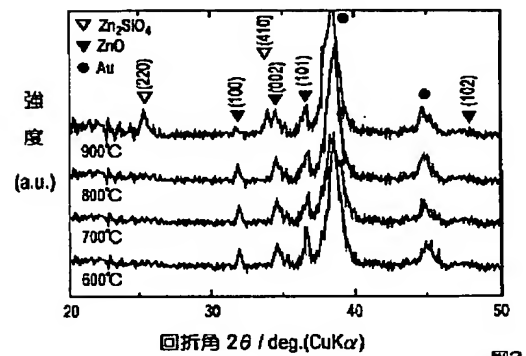


図2

【図3】

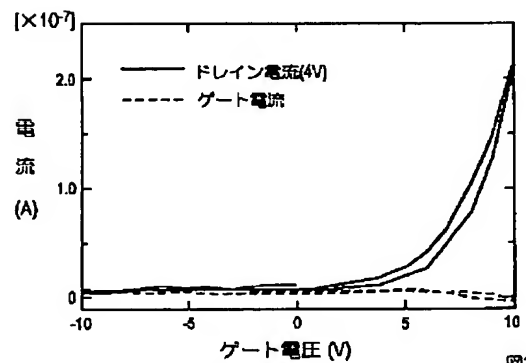


図3

【図5】

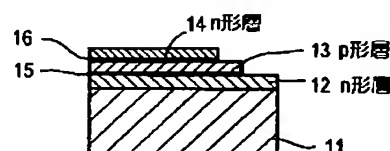


図5

【図 6】

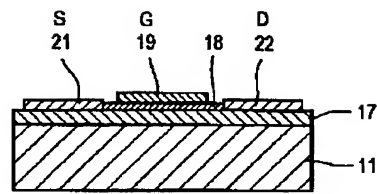


図6

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Fターム(参考) 5F110 DD01 DD03 DD05 DD13 FF03
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H01L 29/786
[FI]
H01L 29/78 618 B
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Epitome

(57) [Abstract]

[Technical problem] FET is produced using a metal oxide semiconductor.
[Means for Solution] It is SiO₂ on the Si substrate 31. Membranous gate dielectric film 32 is formed, after suspending Zn(OAc)₂ and 4H₂O in isopropanol and coating this on gate dielectric film 32, the channel layer 33 which heat-treats and consists of ZnO is formed, and the source electrode 34 and the drain electrode 35 are formed on it.

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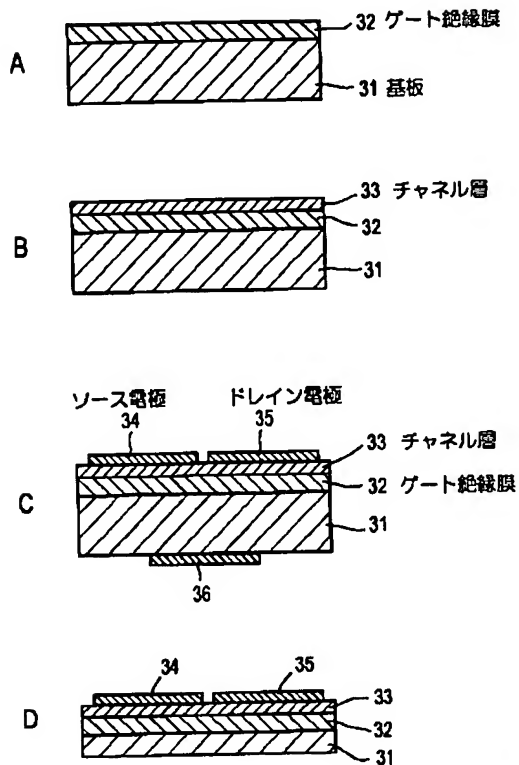


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CLAIMS

[Claim(s)]

[Claim 1] The manufacture approach of the metallic-oxide transistor characterized by forming gate dielectric film on a substrate, making n form or p form metal oxide semiconductor thin film with a solution

method, forming a channel layer on the gate dielectric film, and forming a source electrode and a drain electrode on the channel layer.

[Claim 2] Formation of the channel layer by the above-mentioned solution method is the manufacture approach of the metallic-oxide transistor according to claim 1 characterized by forming the above-mentioned metal oxide layer at comparatively low temperature in the range in which the above-mentioned metallic oxide can deposit, oxidizing the above-mentioned metallic oxide at temperature higher than the above-mentioned temperature after that, and obtaining the above-mentioned metal oxide semiconductor thin film.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the approach of manufacturing the field effect transistor of metal-insulator layer-semiconductor structure using a metal oxide semiconductor.

[0002]

[Description of the Prior Art] As for the conventional transistor, what single crystal silicon is made to diffuse an impurity, and is made to carry out vapor growth, or is made to carry out vapor growth of the compound semiconductor, and forms and manufactures p-n junction is in use. Processing of exhaust gas took a big facility and processing costs in these cases. on the other hand -- sol-gel (Sol-Gel) -- it is possible for there to be no problem of offgas treatment, if a metal oxide semiconductor is produced with the solution method represented by law, and to make cheaply with a comparatively easy facility. However, generally, since mobility was low, the oxide semiconductor had the fault

which is hard to treat as compared with Si, germanium, and a compound semiconductor. Moreover, although the thin film produced by the sol-gel method is porous in many cases and to use the adsorption reaction on the front face of the film like a gas sensor is tried, most electrical conduction phenomena of the thickness direction are not used.

[0003] For example, it is possible to form n form metal oxide layers 12, such as NiO, on a substrate 11, as shown in drawing 5, to form p form metal oxide layers 13, such as TiO, with a solution method on it, to form n form metal oxide layers 14, such as NiO, with a solution method on it further, and to constitute a junction transistor. However, since about 600-800-degree C heating at high temperature is needed for every formation of each metal oxide layer, In case p form metal oxide layer 13 is formed, the multiple oxide film 15 of both layers is generated by the boundary of n form metal oxide layer 12 under it, and p form metal oxide layer 13. Moreover, in case n form metal oxide layer 14 is formed, the multiple oxide film 15 which the multiple oxide film 16 of both layers was generated by the boundary of the n form metal oxide layer 14 and p form metal oxide layer 13, and was moreover previously formed in it grows, and the thickness becomes thick. It is difficult for especially 15 to be unable to become this multiple oxide film and a perfect insulating material, and to be able to move neither in an electron nor an electron hole, but to make it act as a transistor.

[0004] or the channel layer 17 which consists of an n form metal oxidizing zone like NiO on a silicon substrate 11 as shown in drawing 6 -- a solution method -- forming -- the part on the channel layer 17 -- SiO₂ etc. -- forming gate dielectric film 18 with a solution method, forming the source electrode 21 and the drain electrode 22 for the gate electrode 19 on the channel layer 17 in the both sides of gate dielectric film 18 on gate dielectric film 18, and constituting the field effect transistor of M-I-S structure is also considered. In this case, in order not to heat to an elevated temperature after formation of gate dielectric film 18, the multiple oxide film produced on the boundary of the channel layer 17 and gate dielectric film 18 will not become so thick. However, on the channel layer 17, when making gate dielectric film 18 with a solution method, it was difficult to make a good insulating thing.

[0005]

[Problem(s) to be Solved by the Invention] Although the manufacturing facility could make the comparatively easy semiconductor device when producing the metal oxide semiconductor with the solution method as stated above, it was difficult to make a transistor in the former.

[0006]

[Means for Solving the Problem] According to this invention, gate dielectric film is formed on a substrate, on that gate dielectric film, n form or p form metal oxide semiconductor thin film is made with a solution method, a channel layer is formed, and a source electrode and a drain electrode are formed on that channel layer. After formation of the channel layer by the above-mentioned solution method deposits a metallic oxide at comparatively low temperature, it is desirable to oxidize the metallic oxide which deposited at temperature higher than the temperature, and to obtain a metal oxide semiconductor thin film.

[0007]

[Embodiment of the Invention] The example of this invention is shown in drawing 1. The substrate 31 of single crystal silicon (n form, 1.4×10^{-20} ohm-cm) is prepared first, for example (100), and gate dielectric film 32 is formed on the substrate 31. This gate dielectric film 32 oxidizes a substrate 31 thermally, and is SiO_2 . The film can be formed and made. Or it is SiO_2 by sputtering. The film may be formed. Thickness of gate dielectric film 32 is set to 130nm.

[0008] The metal oxide semiconductor thin film of n form or p form is formed with a solution method on this gate dielectric film 32, and it considers as the channel layer 33 (drawing 1 B). for example, this is suspended in isopropanol (a kind of alcohol), using $\text{Zn}(\text{OAc})_2$ and $4\text{H}_2\text{O}$ as an organic metal liquid -- making -- Zn -- receiving -- the diethanolamine of equimolar -- as a hydrolysis retardant -- adding -- dissolving -- further -- the water of 2 double mol is added and the solution of 0.4 mol/l is adjusted. This solution is coated on gate dielectric film 32 with a DIP coating method or a spray method, and a spin coating method. In the case of DIP coating, if a substrate 31 is pulled up at the raising rate for 6cm/out of a solution, the 20nm ZnO film will be formed by one coating, but coating is performed so that the thickness of ZnO , i.e., the thickness of the channel layer 33, may be set to 40nm, for example, and it heat-treats in air or an oxygen ambient atmosphere at the temperature of 600 degrees C - 900 degrees C after that, and forms, the film 33, i.e., the channel layer, of ZnO .

[0009] Next, as shown in drawing 1 C, on the channel layer 33, by the metal membrane, the source electrode 34 and the drain electrode 35 are formed, and a field effect transistor (FET) is obtained. The gate electrode 36 is formed in the gate dielectric film 32 and the opposite side of a substrate 31 if needed. It is good also considering substrate 31 the very thing as a gate electrode. electrodes 34, 35, and 36 -- for example, vacuum evaporation of Au -- or it forms with the solution

method of transparent electrode material, such as ITO (an indium, stannic-acid-ized film).

[0010] The thickness of gate dielectric film 32 has good 500nm or less from the point that channel control is certainly performed from the point that a compound oxide film is generated by the boundary of gate dielectric film 32 and the channel layer 33 although about 100nm or more is desirable. In order to form a channel in contact with the gate dielectric film 32 of the channel layer 33 and for a current to flow through this channel between the source electrode 34 and the drain electrode 35, a current will flow in the thickness direction of the channel layer 33, and a current will flow from an electrode from a channel to an electrode to a channel again. If thickness of the channel layer 33 is set to about 100nm or more from this point, an electronic depletion layer will be made and a current will stop being able to flow easily. Moreover, when it is made about 10nm or less, there is a possibility that the actuation as a channel may stop carrying out good. The thickness of these points to the channel layer 33 has good about 10-100nm.

[0011] When temperature of the heat-treatment at the time of formation of the channel layer 33 is made into 600 degrees C or less, it is ZnO and SiO₂ to the boundary of gate dielectric film 32 and the channel layer 33. Multiple oxide film Zn₂ SiO₄ Since it is not generated enough, the gate current by which the adhesion of gate dielectric film 32 and the channel layer 33 passes along gate dielectric film 32 bad again increases, that is, insulation is bad and good transistor characteristics become difficult to get. Therefore, heat-treatment temperature is made into 600 degrees C or more. On the other hand, when heat-treatment temperature is made into 900 degrees C or more, it is multiple oxide film Zn₂ SiO₄. Thickness becomes thick, the thickness of ZnO (channel layer 33) becomes thin too much, between the source electrode 34 and the drain electrode 35, a current stops being able to flow easily and transistor characteristics are no longer acquired. Oxidation-treatment temperature is made into 900 degrees C or less from this point.

[0012] In the DIP solution of 0.4 mol/l made using said Zn(OAc)₂ and 4H₂O, DIP coating was carried out twice and the line produced FET for heat-treatment 60 minute each, respectively at 600 degrees C, 700 degrees C, 800 degrees C, and 900 degrees C. Heat-treatment is performing DIP coating once, performing heat-treatment for 30 minutes at 600 degrees C after desiccation, performing DIP coating once again, and performing heat-treatment for 30 minutes at 600 degrees C after

desiccation at 600 degrees C here. Each heat-treatment at 700 degrees C, 800 degrees C, and 900 degrees C performed heat-treatment for 30 minutes each twice similarly. Thus, the X diffraction pattern of produced FET is shown in drawing 2 . At 600 degrees C with the low temperature of heat-treatment, it is Zn_2SiO_4 . Although the based peak cannot be checked, the peak based on ZnO is checked. heat-treatment temperature becomes high -- alike -- following -- Zn_2SiO_4 the peak conversely based on [can check the based peak now and] ZnO -- small -- becoming -- 900 degrees C -- Zn_2SiO_4 the based peak -- ***** -- the peak conversely based on [appear greatly and] ZnO -- ***** -- it became small and the peak based on ZnO (100) is lost mostly.

[0013] Although heat-treatment deposits ZnO from these experimental results, it is Zn_2SiO_4 . After performing the low temperature which does not produce generation, i.e., heating by 600 degrees C, depositing ZnO and making it crystallize, heat-treat at 900 degrees C and crystallized ZnO is made to react with SiO_2 (gate dielectric film), and it is Zn_2SiO_4 . It generated thinly. Sum total time amount of both heat-treatment was made into 60 minutes. The X diffraction pattern of the sample in this case became smaller than it when the temperature of the peak based on Zn_2SiO_4 heat-treats only at 900 degrees C. Furthermore, the place, and ZnO and Zn_2SiO_4 which observed the cross section with the transmission electron microscope A clear interface can be observed and they are SiO_2 and Zn_2SiO_4 . And each thickness of ZnO was 115.40 and 45nm, respectively. Zn_2SiO_4 SiO_2 As for the interface, it was also checked very much that it is what has good adhesion.

[0014] It is understood that the technique to which the above thing to heat-treatment makes the semi-conductor which heated and carried out deposit crystallization at temperature higher than this after heating at the oxide-semiconductor crystal and gate dielectric film, and the temperature which does not react and carrying out deposit crystallization of the oxide semiconductor, although the oxide-semiconductor crystal deposited, and gate dielectric film react is desirable. The property over the gate voltage of the drain current and gate current of ZnO -FET which performed heat-treatment for a total of 35 minutes of 600-degree-C each heat-treatment for 10 minutes, and 900-degree-C heat-treatment for 15 minutes by DIP coating twice, and was produced was measured. A continuous line and a broken line show the result to drawing 3 , respectively. There is little leakage (gate current) by the gate electrode from this drawing, and it is understood that transistor characteristics are acquired.

[0015] **** -- setting -- as a substrate 31 -- quartz glass and aluminum

203 etc. -- other ingredients are sufficient. Moreover, SiN₄, SiON, etc. may be used as gate dielectric film 32. furthermore -- as the channel layer 33 -- not only ZnO but TiO₂, BaO, TiBaO, etc. -- you may use -- moreover, not only n form metal oxide semiconductor but NiO and CuO₂, and Co 203 etc. -- p form metal oxide semiconductor may be used. In addition, as shown in drawing 1 D, by cutting or chemical etching, a substrate 31 is shaved for gate dielectric film 32 and the opposite side, and it carries out to below extent to which 0.05mm or less, i.e., the light, penetrates the thickness of a substrate 31, all are removed depending on the case, transparent electrodes (gate electrode), such as ITO, are attached to gate dielectric film 32, and it can make it possible to use it as a liquid crystal drive transistor. That is, it can also be referred to as transparent FET. Moreover, as shown in drawing 4, it is desirable to form an insulator layer with a solution method on a channel layer membrane at least so that the leak current which forms the insulator layers 37, such as silicon oxide and ferroelectric barium titanate, and flows a channel layer front face may be reduced so that it may lap with these periphery sections in part on the forming face of the source electrode 34 and the drain electrode 35 to drawing 1 C.

[0016]

[Effect of the Invention] As stated above, FET which used the metal oxide semiconductor as the channel layer by forming a channel layer with a solution method according to this invention can be produced, and big facilities, such as offgas treatment, are not needed, but it can manufacture with a comparatively easy facility.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The sectional view for explaining the production process of the example of this invention.

[Drawing 2] Drawing showing the X diffraction pattern of ZnO-FET produced at various heat-treatment temperature.

[Drawing 3] Drawing showing the transistor characteristics of ZnO-FET made by this invention approach.

[Drawing 4] The sectional view showing the example of the transistor made by this invention approach.

[Drawing 5] The sectional view showing the junction type metal oxide semiconductor transistor considered with the conventional technique.

[Drawing 6] The sectional view showing the metal oxide semiconductor FET considered with the conventional technique.

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DRAWINGS

[Drawing 1]

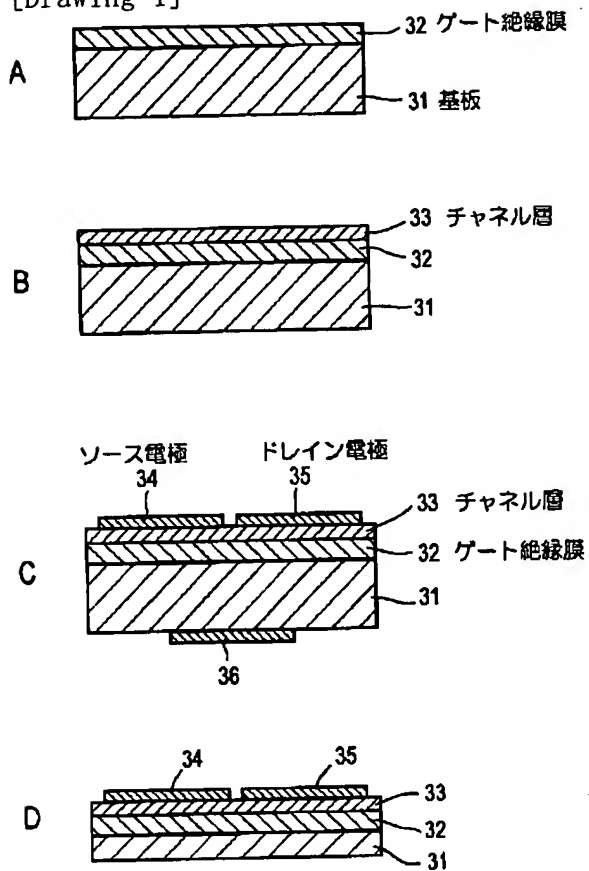


図1

[Drawing 2]

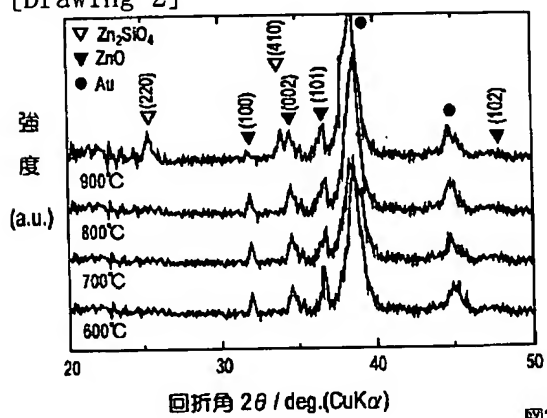


図2

[Drawing 3]

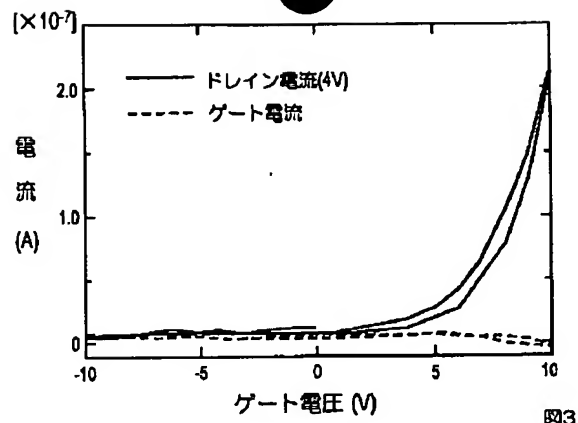


図3

[Drawing 4]

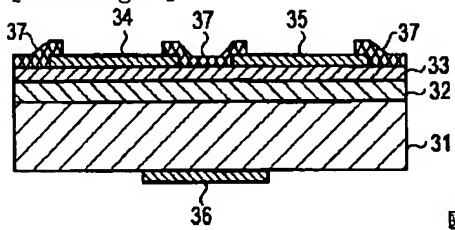


図4

[Drawing 5]

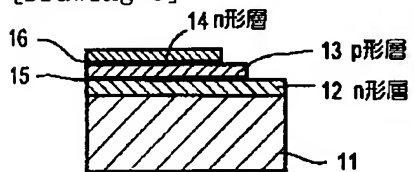


図5

[Drawing 6]

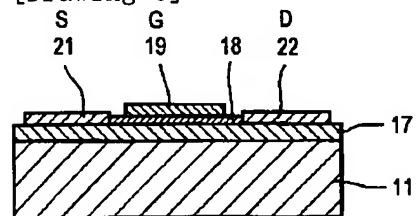


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